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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:

Hideo Akiyoshi

Serial No: 10/056,072

Group Art Unit: 2827

Confirmation No. 3156

Filed: March 26, 2002

Examiner: Trong Q. Phan

For: LATCH CIRCUIT HAVING REDUCED INPUT/OUTPUT LOAD, MEMORY AND SEMICONDUCTOR CHIP

COMMUNICATION TO THE EXAMINER

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Sir:

The present application, claims priority to Japanese Patent Application No. 11-192375 filed on July 6, 1999. A certified copy of the priority document was submitted in the parent application Serial No. 09/610,982 filed on July 6, 2000.

This application was allowed on August 3, 2005. However, the Notice of Allowability does not acknowledge the claim for priority and receipt of the priority documents (filed in the parent application serial no. 09/610,982). However, it should be noted that on the Declaration and on Public Pair, copies of which are enclosed, the Foreign Priority is shown correctly. The Examiner is requested to address this matter, substantially prior to the Issue Fee due date of, November 3, 2005.

Serial No: 10/056,072

If there are questions regarding this communication or the claim for priority, such questions can be addresses by telephone to the undersigned.

Respectfully submitted,

STAAS & HALSEY LLP

Date: August 26, 2005

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LATCH CIRCUIT HAVING REDUCED INPUT/OUTPUT LOAD M
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Application Data	Transaction History	Image File Wrapper	Patent Term Adjustments	Continuity Data	Foreign Priority	Published Documents
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Foreign Priority		
Country	Priority	Priority D
JAPAN	11-192375	07-06-1999

The Patent Electronic Business Center is available to assist with PAIR questions at (8